

DVI Protection Solutions

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The Digital Visual Interface (DVI) specification from the Digital Display Working Group (DDWG) has standardized the means for clocking pixel data discretely to the display panel. DVI provides a standard method to transfer encoded digital data synchronized to a master clock that can be used in LCD and Plasma displays to eliminate the aliasing and image degradation.

Plasma and LCD displays have discrete pixel grids that must match exactly with the X-Y image driven from the video graphics chip. Many of these discrete grid displays include Digital-to-Analog frame conversion logic to synchronize standard analog VGA RGB signals to the X-Y grid.

A very small timing difference between the graphics chip and the frame recapture logic can seriously deteriorate and alias the image quality, as the pixilated image content is interpolated to "fit" the fixed X-Y grid.

The DVI encoding scheme uses "Transition Minimized Differential Signaling" or TMDS, across 4 to 7 differential pairs, as shown in Figure 1. A particular challenge with DVI protection is in limiting digital clock/data skew above and beyond the inherent bandwidth and loading issues of high frequency VGA signals.

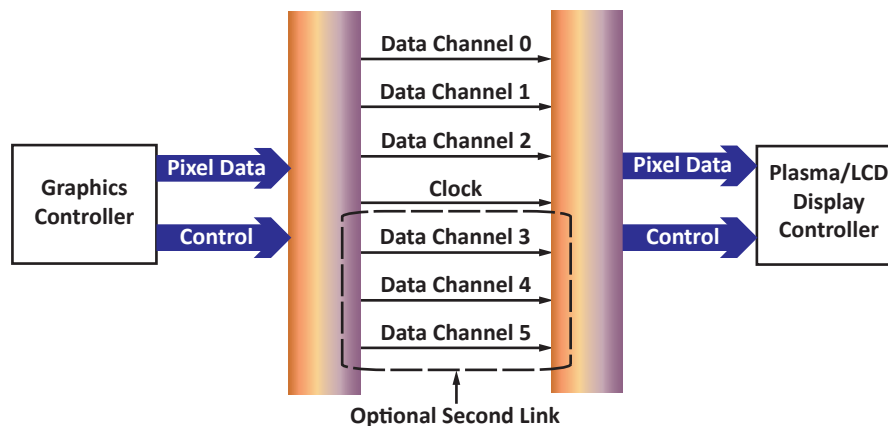


Figure 1. DVI TMDS Encoding Scheme

When both sets of channels are used, odd pixel data are encoded on channels 0-2 and even pixel data are encoded on channels 3-5 (data channels 3 through 5 are optional and may be populated in some applications and are omitted in other lower cost designs). This encoding creates a potential difficulty for protection device partitioning from the 26-pin DVI connector.

The signal channel TMDS configuration requires 4 differential signals (Clock + Channels 0-2) or 8 lines, which need to be protected from transients such as ESD. The dual channel TMDS configuration requires an additional 6 lines of protection for channels 3-5.

Using discrete protection devices of any type can cause imbalances in differential loading, since parasitic load can vary substantially, sometimes by more than their specified tolerances. Figure 2 shows a sample layout for a single channel DVI connector using four PLR0502 devices. By utilizing one PLR0502 on each differential

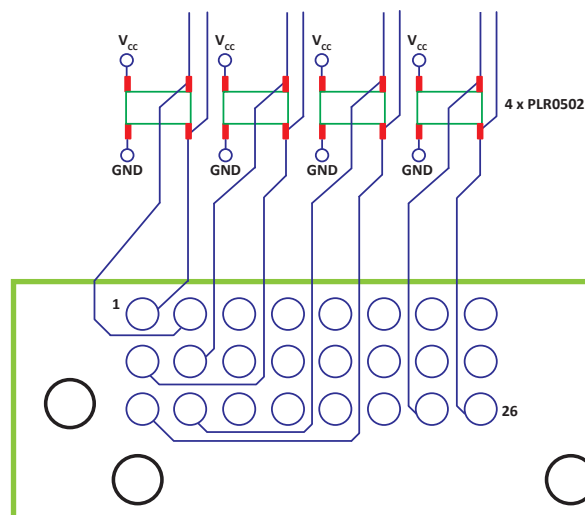


Figure 2. DVI layout using 4 PLR0502 Devices

pair, the close load matching between each (+) and (-) signal, as the devices are fabricated on the same silicon die.

Another method is to use two PLR0504 devices, as shown in Figure 3. This will decrease board space. The quad die is also fabricated on the same silicon thus providing excellent load matching.

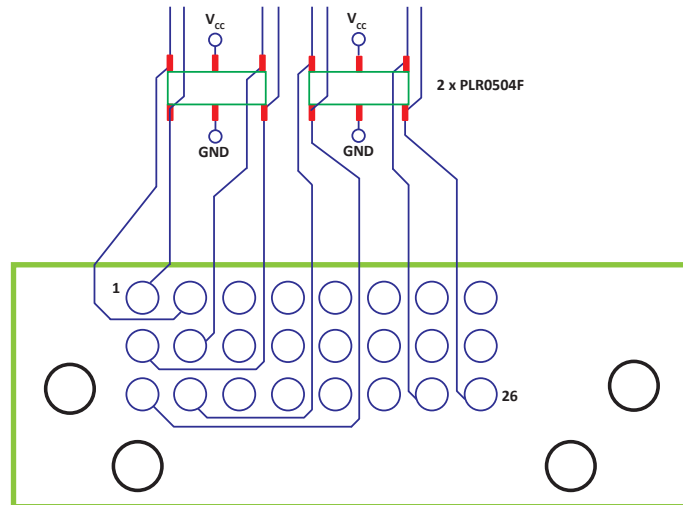


Figure 3. DVI layout using 2 PLR0504F Devices

To maximum channel-to-channel load matching a PLR0508 can be used, as shown in Figure 4.

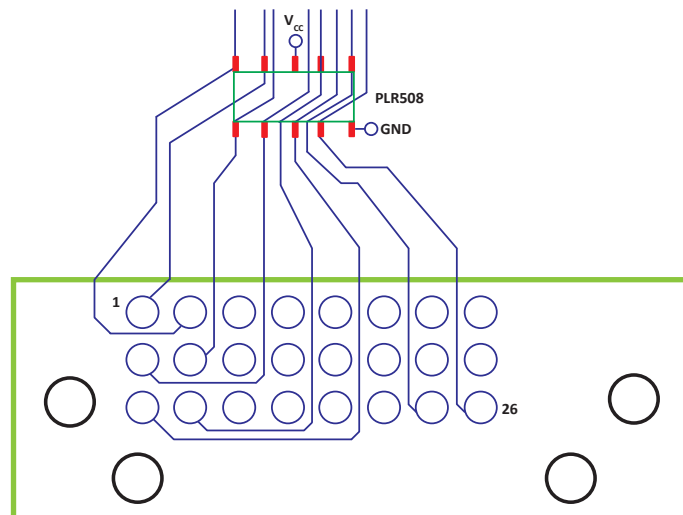


Figure 4. DVI layout using PLR0508

The PLR0502, PLR0504F and PLR0508 provide low clamping voltages, ultra low capacitance, low leakage current, low parasitic load and close port-to-port matching in small package configurations (SOT-543, SC-70-6L and DFN-10 respectively).

COMPANY INFORMATION

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ProTek Devices, based in Tempe, Arizona USA, is a manufacturer of Transient Voltage Suppression (TVS) products designed specifically for the protection of electronic systems from the effects of lightning, Electrostatic Discharge (ESD), Nuclear Electromagnetic Pulse (NEMP), inductive switching and EMI/RFI. With over 25 years of engineering and manufacturing experience, ProTek designs TVS devices that provide application specific protection solutions for all electronic equipment/systems.

ProTek Devices Analog Products Division, also manufactures analog interface, control, RF and power management products.

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