Understanding I/O Port Protection

By: ProTek Devices

With the increase in the number of immunity standards, selecting a protection device for I/O port protection has become a very challenging process for the design engineer. Not only must the protection device be compatible with the standards, it must also be capable of conducting/diverting the transient current, clamp threats to their lowest voltage, and be properly packaged in accordance to its location on the printed circuit board (PCB). Then there is the issue of cost effectiveness.

The good news is that a TVS can meet these requirement and provide the design engineer with some latitude in design. Moreover, with the proper selection and placement of a TVS device, additional problems such as EMI/RFI from conducted or radiated disturbances can be prevented.

STAGES OF DESIGN

In the preliminary stages of design, the engineer begins with the selection of the IC components that are necessary to perform a defined system function. The IC component selection process also includes an appropriate interface (I/O port) circuit or IC transceiver. In turn, the interface circuit has certain standards that must be met and taken into consideration by the designer. After the components have been chosen, the circuit operating parameters (signal operating voltage and frequency) become more evident. The TVS has parameters (capacitance, stand-off voltage, peak pulse current) that need to be taken into account to be compatible with circuit performance of the EMC environment.

Circuit Configuration

Interface circuits can be divided into two basic configurations - balanced lines and unbalanced lines. As shown in Figure 1, a typical unbalanced line configuration consists of a line driver and a line receiver or a transceiver connected to a data transmission line. An unbalanced line uses the ground as the circuit return

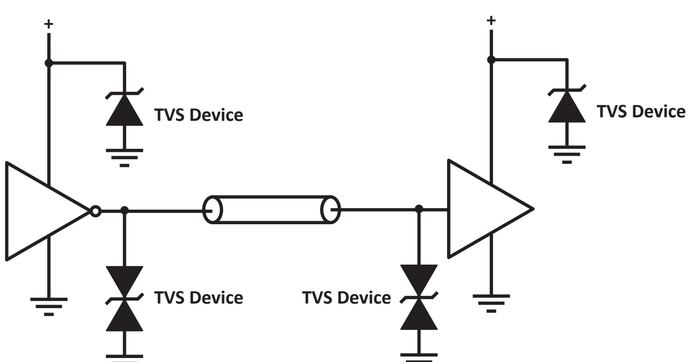

Figure 1. Unbalanced data line configuration showing TVS protection on the I/O ports and the DC power bus lines.

path. For some applications, there will be multiple unbalanced line transceivers in a given IC package requiring multiple TVS device protection. Unbalanced lines can be more challenging in providing protection due to the different types of transient threats - ESD, lightning, noise.

A typical balanced line configuration, as shown in Figure 2, is comprised of differential I/O ports in which the ground is separate and not used as a signal return path. The ground is typically connected to the IC component through the ground plane (trace) of the power bus at some single point location. However, due to common-mode interference, it is important to have data line protection from

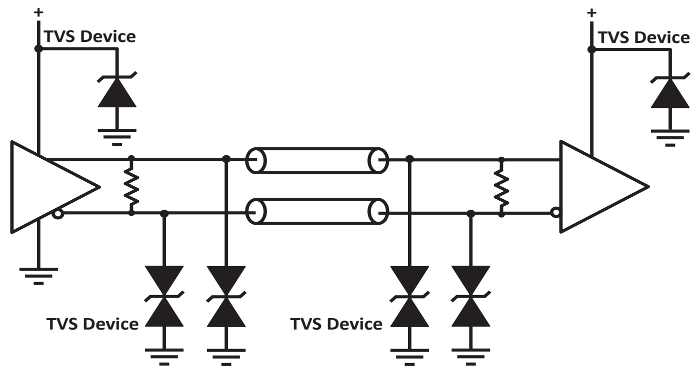

Figure 2. Balanced data line configuration showing TVS protection on the I/O ports and the DC power bus lines.

each line to ground and from the power bus to ground.

Data lines will always require common-mode protection for transient threats such as electrostatic discharge (ESD) or induced lightning. In some cases, data lines will require differential-mode protection to protect against electrical fast transients (EFT) or other switching transients. If a switching transient becomes significant in magnitude, a TVS may be used between transmit and receive lines. A TVS placed across both lines to ground is sufficient in most circuit applications.

Although TVS device selection is similar for both types of interface circuit configurations, there are some differences in the number of protection devices require.

Standards & Parameters

Interface standards such as RS-485, Ethernet, FireWire, USB and SCSI (to name a few) define circuit performance and provide information for IC component selection. Interface standards determine the circuit's data rate and signal operating voltage. From this information, key parameters associated with the selection process of a TVS can be defined. Without knowledge of the above parameters, protection at board level will be hit and miss at best.

For a circuit to be consistent with interface standards, TVS device capacitance should be taken into consideration. Capacitance is based primarily on operating frequency and parasitic capacitance is based on transmission line distance. To much line capacitance can distort the leading edge of a digital pulse and reduce the peak value of the signal below the required voltage limit.

Immunity standards such as IEC, EM, EOS/ESD, ANSI, IEEE, Bellcore and ITU provide the engineer with the voltage, current and waveshape parameters of the transient threat. For example, ANSI/IEEE C62.41, a standard for identifying lightning transients, provides a good estimate of peak pulse current ratings for short pulse durations using an 8/20µs or 10/1000µs waveshape. Understanding the waveshape is important when selecting a TVS device.

Testing and Placement

Unfortunately, most TVS specifications do not provide the transient current ratings for fast rise time transient events such as ESD or EFT. Both of these transients can present a significant threat to board level components. For instance, ESD can occur in the tens of thousands of volts within a few nanoseconds. Protection is best determined by an in-circuit transient test.

Matching circuit parameters, immunity and interface standards to TVS device parameters is only part of the story. Optimal placement of a TVS is essential for effective protection and circuit performance. Typically, problems occur when the circuit is tested to a specific transient immunity standard and the TVS is found to be improperly placed (if it is there at all) on the printed circuit board. This can cause significant voltage differentials between data lines or ground points. Compliance testing a circuit design after all the components, layout circuitry and interconnects are in place can be a costly mistake. A good rule of thumb is to review the circuit layout at designed frequencies to determine problems areas before they occur. It is also recommended that an EMI/RFI analysis be conducted before and after component placement and trace routing have been identified on the PCB.

Transient threats at the I/O port interface are either tertiary lightning, internal switching or ESD. TVS device placement is determined by the source of the transient threat. For instance, a discrete TVS may be more appropriate for protection at the individual components when protecting against internally generated threats which are generally low level and very fast. Internal sources of these types of threats are attributed to high-speed cloaks, fast (digital) signals and poor grounding, where external sources are linked to long signal lines and sometimes poor grounding.

EMI/RFI disturbances can also be a potential threat if the circuit is not properly laid out for minimum noise pickup. EMC sources have been attributed to high speed clocks, fast signals, long signal lines and poor grounding. Electromagnetic radiated voltages generally come from onboard loops in PCB traces. When these transient (noise) sources exceed the withstand level of the IC component, they can cause malfunctions in the circuit. For this type of situation, a TVS should be placed adjacent to the IC component.

When inadequate grounding is a concern, the placement of the TVS should always be in reference to a low impedance ground return path. This type of ground path is most likely used as the return path for the transient current. For example, common-mode threats such as lightning and ESD are referenced to low impedance ground whether it is a chassis or a PCB ground plane.

It is important to design a ground system (path) with a minimum number of discontinuities for reducing common-mode radiation. In applications where there are both analog and digital signals without a common ground, a low voltage TVS device should be used between two grounds to prevent significant voltage differentials between grounds. The TVS should also be higher in voltage than the operating voltage of the two signals.

Placing a TVS at the card edge aids in keeping both the input and the output lead traces to a minimum and provides both I/O and power bus protection. This will also minimize the introduction of radiated emissions onto the PCB during a transient event. The number of I/O ports that need to be protected will determine the TVS device package configuration. For example, a one line device would be adequate for a single I/O port. A multi-line TVS array would protect multiple I/O ports.

SUMMARY

There are many variables an engineer must take into consideration during the design stage. The best TVS device is one that will meet industry standards, immunity standards and circuit operating parameters. The following are general guidelines that will reduce the trail and error process:

1. TVS device capacitance should be consistent with the frequency (data rate) of the operation.
2. Frequency response or insertion loss should be less than 1db at operating frequency.
3. The peak pulse transient current should be less than the maximum handling current of a TVS.
4. The circuit operating voltage should be less than the stand-off voltage of the TVS device.

COMPANY INFORMATION

COMPANY PROFILE

ProTek Devices, based in Tempe, Arizona USA, is a manufacturer of Transient Voltage Suppression (TVS) products designed specifically for the protection of electronic systems from the effects of lightning, Electrostatic Discharge (ESD), Nuclear Electromagnetic Pulse (NEMP), inductive switching and EMI/RFI. With over 25 years of engineering and manufacturing experience, ProTek designs TVS devices that provide application specific protection solutions for all electronic equipment/systems.

ProTek Devices Analog Products Division, also manufactures analog interface, control, RF and power management products.

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