PROTEK DEVICES
Analog Products Division

P.A.NOTES #11

High Speed USB Design Guide:

Terminology

- Clock; - A periodic signal, (as defined for EMC purposes) above 10MHz.
- PCB; - Printed circuit board
- EMC; - Electromagnetic Compatibility-The condition which prevails when electronic equipment/systems,
- Collectively perform their individually designed functions in a common electromagnetic environment without causing or suffering unacceptable degradation due to EMI to or from other electronic equipment/systems in the same environment.
- EMC can be broken down to two major subcategories, emissions and immunity, with ESD being a subcategory of immunity.
- EMI; -Electromagnetic Interference, the opposite condition of EMC in which a piece of ITE causes or suffers unacceptable degradation to or from other electronic equipment in the same environment.
- ESD; -Electrostatic discharge.
- HS; -High speed, USB signaling at 480Mb/s (Mega bits per second).
- FS; -Full speed, USB signaling at 12Mb/s.

Board design guidelines

- Specific requirements concerning routing and placement of the host controller recommended trace separation, termination placement requirements and overall trace length guidelines are provided.
- These are followed by general guidelines concerning plane splits and layer stack-up.
- Some examples of common routing mistakes are also included to show the designer some suggestions about what to avoid when routing USB signals.

EMI/ESD guidelines

ESD solutions are provided based on actual testing.

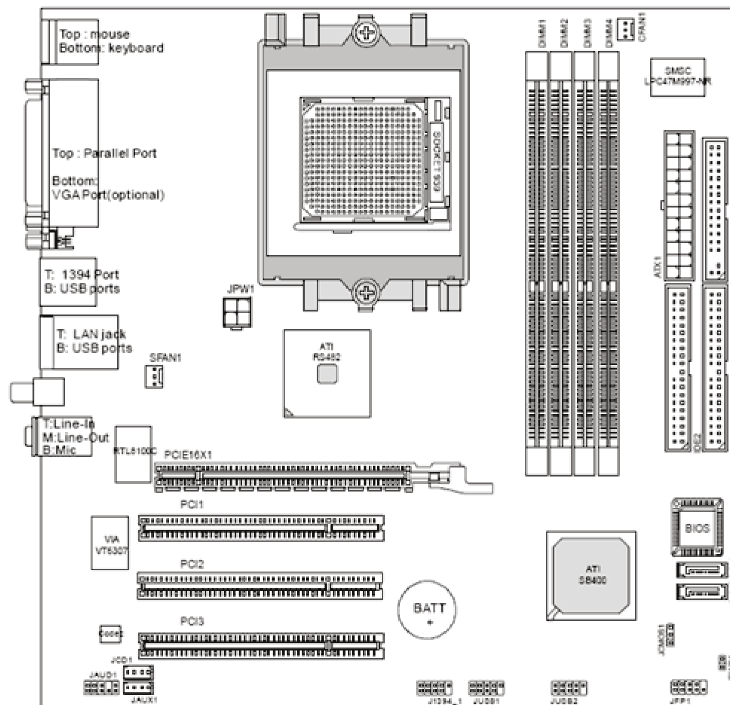

Fig.1 Typical Motherboard Layout

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General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design.
These guidelines will help to minimize signal quality and EMI problems. The high speed USB validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer.
This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

- Place the high-speed USB host controller and major components on the un-routed board first. With minimum trace lengths, route high-speed clock and high-speed USB differential pairs first.
- Maintain maximum possible distance between high-speed clocks/periodic signals to high speed USB differential pairs and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route high-speed USB signals on bottom whenever possible.
- Route high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.
- Route all traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferable to change layers to avoid crossing a plane split.
- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
- Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (V_{CC} or GND, depending on the plane the trace is over).
- For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

High Speed USB Trace Spacing

Use the following separation guidelines. Figure 3 provides an illustration of the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90Ω differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of deviations is kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. For the board stack-up parameters referred to in section 3.7 Layer Stacking, 7.5mil traces with 7.5mil spacing results in approximately 90 ohms differential trace impedance.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. The recommended minimum spacing to clock signals is 50 mils.
- Use 20mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps prevent crosstalk.

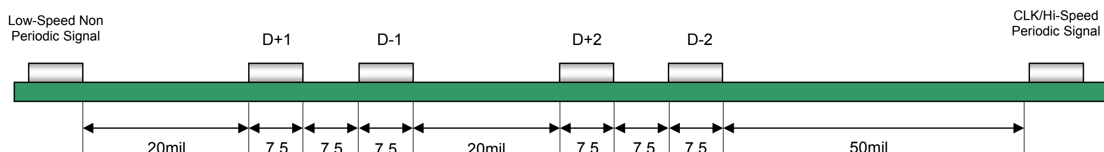

Fig.2 Recommended trace spacing (in mils) for USB traces

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High Speed USB Termination

Use the following termination guidelines.

- High-speed USB designs require parallel termination at both the transmitter and receiver. For host controller designs that use external termination resistors, place the termination resistors as close as possible to the host controller signal pins. Recommend less than 200mils if possible. Follow the manufacturer's recommendation for the termination value needed to obtain the required 45Ω to ground parallel HS termination.
- For downstream ports, a 15 kΩ pull down resistor on the connector side of the termination is required for device connection detection purposes. Note that this pull down might be integrated into the host controller silicon. Follow the manufacturer's recommendation for the specific part used.
- A common mode (CM) choke should be used to terminate the high speed USB bus if they are needed to pass EMI testing. Place the CM choke as close as possible to the connector pins.

Note: Common mode chokes degrade signal quality, thus they should only be used if EMI is a known problem.

High Speed USB Trace Length Matching

Use the following trace length matching guidelines.

High-speed USB signal pair traces should be trace-length matched. Maximum trace-length mismatch between
USB signal pairs (such as, D- and D+) should be no greater than 150mils.

Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits, voids and cutouts.

VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the V_{CC} plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to High Speed USB signals, high-speed clocks and signal traces as well as slower signal traces, which might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode)
- Avoid routing of USB signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.
- When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one and the other.
- If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1μF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split.
- They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates V_{CC5} and V_{CC3}
- Planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to V_{CC5} and the other side should tie to V_{CC3}. Stitching caps provide a high frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)
Use the following guideline for the GND plane.
- Avoid anti-etch on the GND plane.

Layer Stacking
The following guidelines apply to PCB stack-up.

Four-layer Stack-Up
1. Signal 1 (top)
2. VCC
3. GND
4. Signal 2 (bottom, best layer for USB2)

A high speed USB motherboard uses 7.5-mil traces with 7.5-mil spacing between differential pairs to obtain 90Ω differential impedance. The specific board stack-up used is as follows:
- 1 ounce copper
- prepreg 4.5 mils
- core 53mils
- board thickness 63mils
- _r 4.5 (relative permittivity)

Component Placement
The following guidelines apply to component placement on the PCB.
- Locate high current devices near the source of power and away from any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors.) This reduces the length that the return current travels and the amount of coupling to traces that are leaving the PCB.
- Keep clock synthesizers, clock buffers, crystals and oscillators away from the high speed USB host controller, high speed USB traces, I/O ports, PCB edges, front panel headers, power connector, plane splits and mounting holes. This reduces the amount of radiation that can couple to the USB traces and other areas of the PCB.
- Position crystals and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under crystals and oscillators having multiple via's connecting to the ground plane. These will help reduce emissions.

Some Common Routing Mistakes
Stubs
A very common routing mistake is shown in Fig.3 the designer could have avoided creating unnecessary stubs by proper placement of the pull down resistors over the path of the data traces. Once again, if a stub is unavoidable in the design, no stub should be greater than 200 mils.

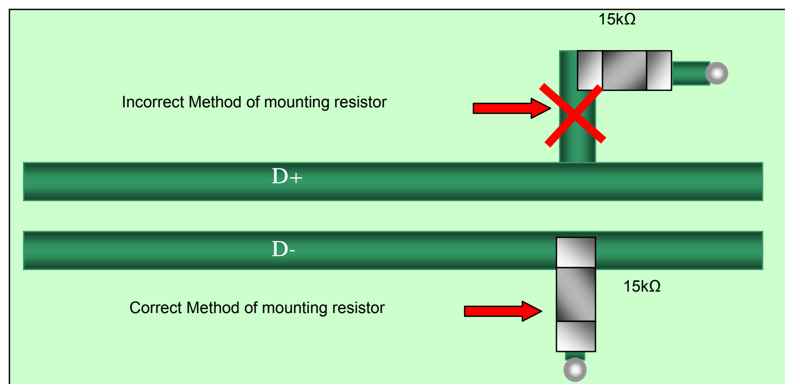

Fig.3 creating unnecessary "stubs"

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Poor Routing Techniques
Fig.4 demonstrates several violations of good routing practices for proper impedance control and signal quality of high speed USB signaling.

Crossing a plane split
The mistake shown here is where the data lines cross a plane split. This causes unpredictable return path currents and would likely cause a signal quality failure as well as creating EMI problems.

Creating a stub with a test point
Here is another example where a stub is created that could have been avoided. Stubs typically cause degradation of signal quality and can also affect EMI.

Failure to maintain parallelism
Fig.4 is also a classic example of a case where parallelism was not maintained, when it could have been. The orange trace shows the wrong way to route to the connector pins. The green trace (the darker trace in the middle) shows the correct way. Failing to maintain parallelism will cause impedance discontinuities that will directly affect signal quality. In this case it also contributes to the trace-length mismatch and will cause an increase in signal skew.

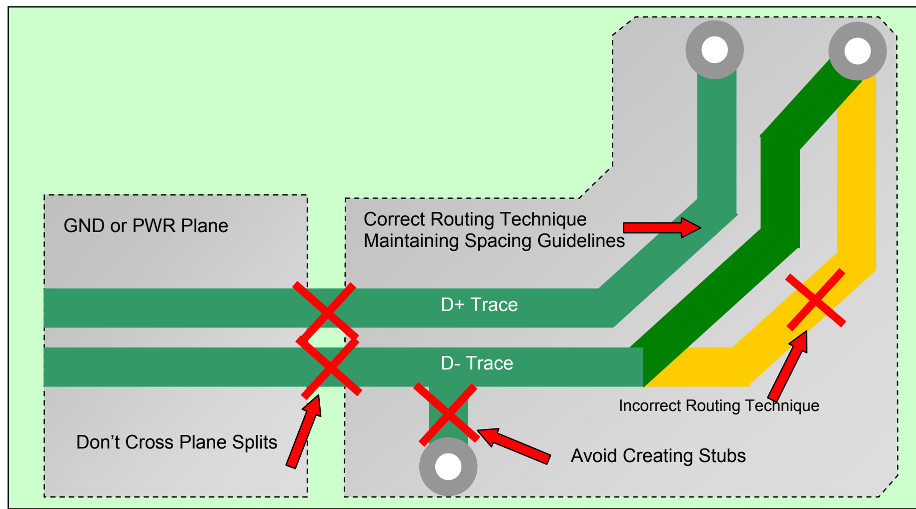

Fig.4 Violation of proper routing techniques

EMI/ESD Considerations
The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

EMI - Common Mode Chokes
Common mode chokes can provide required noise attenuation. A design may include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing.
Fig.5 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins

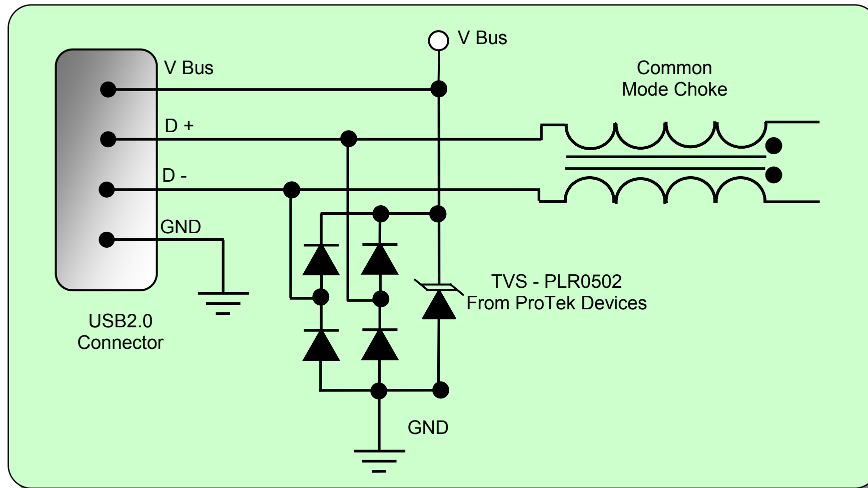

Fig.5 Common mode choke

ESD

Low-speed and full-speed USB provide ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique doesn't work for high speed USB due to the much higher signal rate of HS data.

A device that has been tested successfully is the PLR0502 a combination of steering diodes and TVS available from ProTek Devices. The capacitance of each protection line is rated at 0.6pF line to ground. Proper placement of the device is on the data lines between the common mode choke and the USB connector data pins as shown in Fig.5

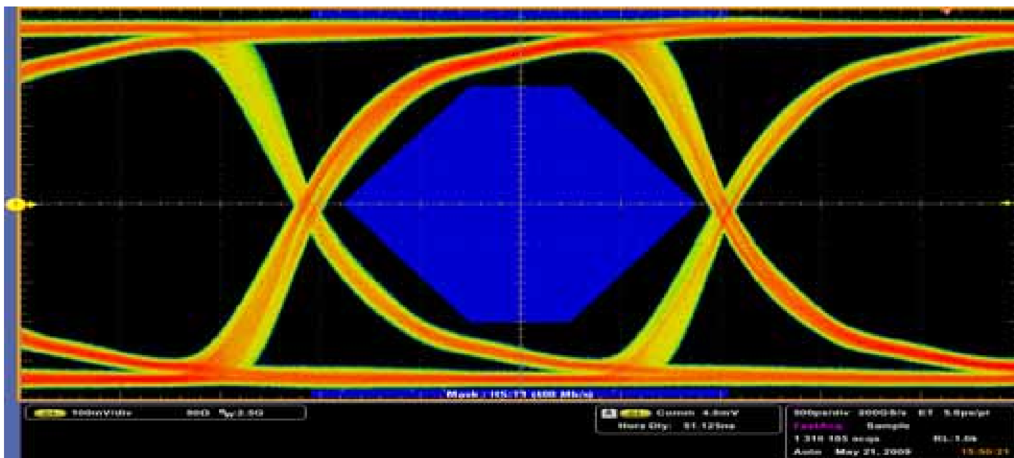

Fig.6 Eye Diagram
This is showing compliance to USB2.0 Standards. (480Mb/s High Speed) of the PAUSB42 DPDT switch

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