# ESD Standards vs Real-World Conditions

*By: ProTek Devices*

Electrostatic Discharge (ESD) is a well-known transient threat to sensitive IC components, products and systems. The ESD association has estimated the average loss of product due to user-generated ESD at 27% to 33%.[1] It continues to be the primary cause of component and product failure, costing the industry billions of dollars per year.[2]

Yet, despite ESD's notoriety, its maximum voltage and current values with regard to real-world transient conditions are poorly understood. Studies have been done to determine the level of static charge a person can pick-up by walking across a carpet. Voltages up to 40 kilovolts have been recorded under special conditions.[3] Typically, the charge build-up from a human body ranges from 20kV to 30kV, depending upon the relative humidity of the air and type of clothing material being worn.

Curiously, industry standards developed from factory floor and field failures do not reflect these studies. IEC characterizes ESD contact discharge at 8kV and air discharge at 15kV.[4] These do not represent real-world conditions. As IC components employ smaller geometry and higher integration; components, products and systems become more susceptible to ESD. Design engineers must deal with real-world ESD threats at the design stage by understanding potential voltage and current values, waveforms, components and product susceptibility levels, points of entry and external protection components or networks as they apply to the end user.

## DEFINING ESD

Think of Electrostatic Discharge as a miniature lightning event, where an electrical charge is transferred between two surfaces or objects that are differing potentials. The build-up of an electrical charge is called tribocharging or triboelectric generation.[5] When a charged object approaches or touches another conductive object, an arc will occur causing an uncontrolled transfer of charges. ESD is a single, fast, high voltage and high current event resulting from the near or direct contact of two objects generating both an electric and magnetic field.

Electrostatic Discharge is defined by three models; Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM).

### *Charged Device Model (CDM)*

A static charge can accumulate on a device through handling or contact with packaging materials or work surfaces. This frequently occurs when a device moves across a surface or vibrates in a metal tray. The model used to simulate the transfer of charge between two devices is referred to as the Charged Device Model (CDM).

### *Machine Model (MM)*

Similarly, Machine Model (MM) refers to the accumulation and transfer of a charge from equipment to equipment.

### *Human Body Model (HBM)*

The Human Body Model (HBM) is the most prominent source of ESD, where simple human contact or air discharge can cause component or product failure on fixed or handheld equipment.

There are two kinds of HBM ESD standards. The first originated from the need to define ESD's withstand level for IC component susceptibility during manufacturing, packaging and handling. Figure 1, shows a storage capacitor is charged in steps from 500 Volts up to 4000 Volts for both polarities. Although voltage is the

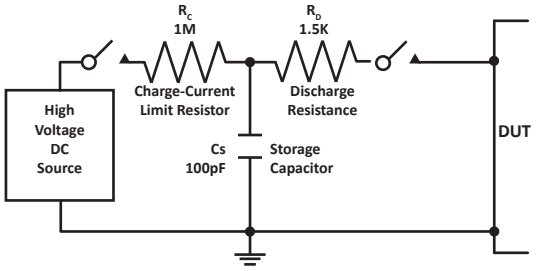


**Figure 1. Test Circuit for HBM ESD, MIL-STD-883, Method 3015**

trigger or root cause and can breakdown some CMOS structures, it is the current that causes most of the physical damage. Through the R/C network, a current source is injected into the Device Under Test. The current waveform for this test is shown in Figure 2. The purpose of this test is to determine the component ESD failure threshold classification and is used to understand the precautions necessary for manufacturing, packaging and handling sensitive IC components.

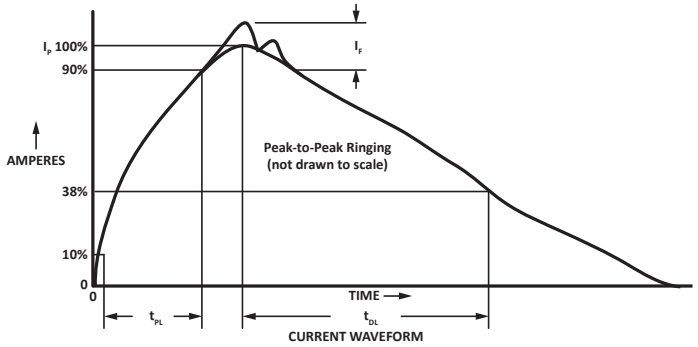


**Figure 2. Human Body Model Current Waveform for MIL-STD-883, Method 3015**

The second HBM standard was developed to define potential levels of exposure to products and systems by users through either contact or air discharge (IEC 61000-4-2). The objective of this EMC immunity standard was to determine the susceptibility of products or systems to HBM ESD. Although the document has not change in content, the standard has gone through three document number changes: IEC 801-2 1984, IEC 1000-4-2 and currently IEC 61000-4-2. The standard was largely developed from the work of CENELEC, the European standards organization. Once approved by IEC, Europe adopted the standard and changed the number to EN61000-4-2. The EN(Euronorm) standard is in force by a directive from the European standards board to ensure fair trade between various countries.

There were several assumptions made in developing the test and circuit waveform for the IEC standard.[6] Figure 3 represents the surge generator and

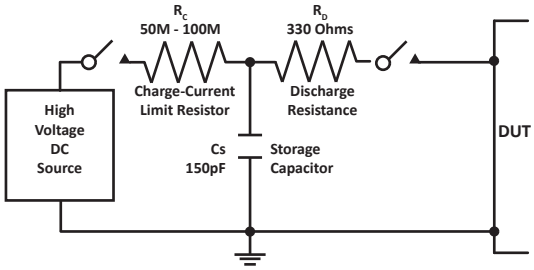


**Figure 3. Test Circuit for HBM ESD for IEC 61000-4-2**

discharging R/C network. There is a significant difference in the series discharge resistor between MIL-STD-883 and IEC 61000-4-2. MIL-STD-883 has a discharge resistance of 1500 Ohms, while IEC has a discharge resistance of 330 Ohms.

This difference was an attempt by IEC to define the combined resistance of the human body holding a hand-held tool. As with the MIL-STD document, voltage is the trigger, but the peak pulse current causes most of the damage. As a result, the discharge waveform is represented by the current waveform. However, specific voltage levels are defined for each peak current value.[7] As shown in figure 4, the initial peak current (< 10ns) represents the discharge of the tool while the second peak current represents the balance of the discharge of the human body.

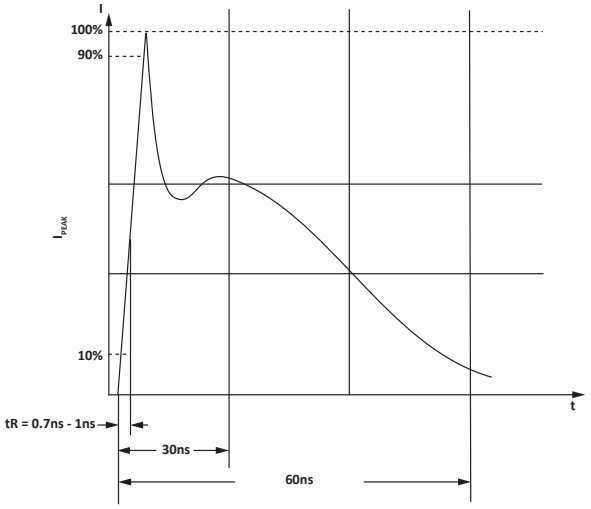


**Figure 4. Current Waveform for HBM ESD for IEC 61000-4-2**

As stated earlier, these values do not accurately define real-world ESD potentials. In the 1960s, Sandia Labs measured ESD discharged from a human body. Under the right conditions, a human body can be charged up to 40 kilovolts of ESD and dissipating up to 80 Amps.[8] Other examples include walking across a carpet, sliding across a seat in an automobile, rubbing clothing against chairs where there is little to no humidly. In these cases, there is a high probability of generating a high voltage ESD event (20kV to 40kV).

Semiconductor device failure studies from various sources have indicated that most real-world ESD failure signatures fit the HBM ESD events. These results are reflected in the ESD standard. However, there is no standard that represents real-world conditions for ESD.

## ESD PROTECTION MEASURES IN THE MANUFACTURING PROCESS

IC component manufacturers employ integrated ESD protection networks in order to meet industry standard requirements. ESD can affect the component at any stage of processing - from fabrication, assembly, testing and handling, all the way through shipment. To protect components during this process, IC manufacturers utilize "On-Chip" protection and manufacturing floor controls.

Most of these manufacturers will employ some type of protection network on the semiconductor chip at specified ports with some test condition restrictions. Generally, this applies to specific ESD withstand voltage levels and the pins that are to be tested. In addition, precautions such as wrist straps, ESD protective clothing, footwear, static-dissipative flooring or mats, are employed to control ESD on the manufacturing floor.

Although IC component manufacturers meet industry standard requirements for the manufacturing process, they have achieved limited success at meeting real-world ESD transient threats. The maximum ESD protection level for IEC 61000-4-2 contact discharge is 8kV and 15kV for air discharge. These levels are inadequate when required to protect against 25kV to 40kV of static discharge caused by a person walking across a carpet with rubber soles. After all, not many SMART phone users are going to wear ESD protective gear while using their device.

## END-USER ESD PROTECTION

"On Chip" protection and other ESD controls may be adequate protection during the manufacturing process, but what about the end user? IC pins that are exposed to the external environment can encounter high levels of ESD, even when mounted inside an enclosure. Coordinating all pins and ports that include I/O (data and control) and power bus inputs, with an external protection network has become necessary for total ESD protection.

### *External Protection Networks*

The peak voltage characteristic of an ESD pulse is often the trigger, causing short or low impedance paths between the voltage bus and the ground. It is also recognized that the peak pulse current can cause some physical damage. Depending upon the current duration due to some series impedance, a transient current as low as 3 Amps can cause rapid melting of chip metallization and other interconnect layers. Peak currents can radiate EMI/RFI, affecting other internal sensitive ports. ESD voltage and current should be limited at key interface points rather than at the sensitive IC component. External protection components or networks are effective in these situations.

There are several discrete components and networks that provide ESD protection. Some external protection components are spark gaps, polymer suppressors, metal oxide varistors (MOV), multilayer varistor (MLV), transient voltage suppressor diodes (TVSD), steering diodes and integrated diode/filter networks. Each of these solutions has their pros and cons.

### *Spark Gap*

The most difficult to design and control is the spark gap, that is sometimes used on a PCB. Whether designed with two point contacts or interdigitated structures, the gap can widen or become charred to the extent that the gap will no longer breakdown at its designed value.

### *Polymer Suppressor*

Polymer Suppressors employ a type of dielectric between two metal contacts. These devices are used on high frequency antennas, which can be exposed to ESD. The advantages of this device is its low capacitance and low voltage after the initial strike voltage. The disadvantages are a high striking voltage (~100 to 300 Volts), current handling capability and an increase in leakage current after several ESD events.

### *Metal Oxide Varistor (MOVs)*

The standard Metal Oxide Varistor (MOV) device was originally designed for AC power line protection on commercial products. Due to their high current handling capability, high protection voltage and low cost, they still have the advantage over other technologies for AC power line applications. However, some major disadvantages are high leakage current, high capacitance and degradation after several ESD events.

### *Multilayer Varistor (MLV)*

The Multilayer Varistor (MLV) is a newer version of the MOV. Similar to an MOV but lower in voltage and cost. However, due to higher on-resistance, the clamping voltage is still high for some IC components. Other disadvantages include high leakage currents, high non-linear capacitance and degradation after several ESD events.

### *Transient Voltage Suppressor Diode (TVSD)*

Discrete transient voltage suppressor diodes (TVSD) were initially introduced in 1968 for the protection of solid-state telecommunication line equipment (repeaters). They were robust in their design; effectively clamping secondary induced lightning effects and diverting significant transient currents to ground. In addition, its clamping voltage and current handling capability, allowed the design engineer the freedom to place the device at key interface points. The TVSD has successfully made the transition from a device that protects only against the secondary effects of lightning, to a device that also protects against switching transients, electrical fast transients (EFT) and electrostatic discharge (ESD).

Due to better characterization of the transient environment, TVSDs have been redesigned into smaller packages including chip-scale configurations. The smaller TVSD components were designed for both EFT and ESD protection at the PCB level; whereas the larger components were designed for longer duration transient events. Smaller components have kept pace with the increased digital data rate transmission applications through the addition of a compensating rectifier diode to lower capacitance. The advantage of this diode combination over other techniques of capacitance compensation is the linearity of the capacitance over the operating voltage range of the circuit. Other techniques employing smaller components such as bridge rectifier networks, will have varying capacitance values over the operating voltage range. The advantage of TVSD devices is that they provide low clamping voltage, low leakage current and low capacitance. In addition TVSD components have no power-down issues and are available in a variety of multiple array configurations.

### *Steering Diodes*

Steering diode configurations or dual forward diodes are connected to the data line between the power rail and ground. Due to trace layout on the PCB, a parasitic series inductance is created from the steering diode to the power bus. This inductance will resist rapid changes in the peak pulse current of the ESD event often causing the transient current to be shunted into the IC component. A series resistor between the dual steering diodes and the input to the IC component is then required. This means an additional external component or if integrated on the semiconductor chip, means less real estate for the protection network. Where this may be acceptable on some input pins, it is not generally used on output pins without causing some insertion loss. An additional problem with steering diodes is that if the power bus is brought to ground when powered down, the driver circuit on the other end of the line will supply current directly to ground. This can cause high current dissipation, draining batteries and may cause physical damage to the peripheral devices. The advantage of steering diodes is their low capacitance for high-speed data rate applications. However, ti is best to use this type of protection on low voltage applications (< 1 Volt), as the capacitance will increase with the higher voltages in the forward direction.

### *Integrated TVS Diode/Filter Network*

TVS diodes are being integrated with R/C components to provide ESD protection and low pass EMI/RFI filtering within a single component. The TVSD serves as one leg of a pi network. Some designs use two TVS diodes on either end of a series resistor to form the pi network. In effect, this type of network serves to offer ESD protection from either direction and filters high frequency EMI/RFI noise. EMI/RFI filtering and ESD protection are being used more and more on data ports at the IC component interface rather than at key interface ports. This is due to the filtering advantage of the network for radiated EMI/RFI noise within the system. Additional advantages of a TVSD/Filter network include reduced number of components (board-space saving), lower cost and combined functionality (ESD immunity plus EMI/RFI Filtering).

## OPTIMUM PLACEMENT OF TVSD PROTECTION DEVICES

To terminate ESD at its source would require people to wear wrist straps tied to earth ground. This would be a highly ridiculous solution. The best alternative is to determine a point of entry that can be defined as an interface location, such as a building entrance for lightning, motor or relay connector terminals or printed circuit board ports. A point of entry is basically defined as the location where an ESD pulse can be coupled to a low impedance return ground and where it will generate the least amount of EMI/RFI. Protection at these entry points will divert the current pulse so that the electric and magnetic fields will not couple into the surrounding components. It is recommend that all I/O ports have one general entry point at the product connector or PCB card edge to minimize the effects of ESD.

Due to the nature of EMI/RFI, metal enclosures or shielding are recommended to reduce the effects of ESD propagating electric and magnetic fields on the PCB cards. For instance, plastic enclosures, manufactured with special types of paint, laminate or plating can limit the effects of radiation. Similarly, the optimal placement of a TVS diode will create a low impedance path to ground the flow of ESD current away from sensitive components and reduce the effects of both electric and magnetic fields from EMI/RFI affects.

As a rule of thumb, use ground planes, metal straps or wide PCB traces to conduct ESD pulses back to the source. The low impedance may be a direct ground connection or a by-pass capacitor connected to ground.

It is important to connect the chassis to ground to a connector or cable entry point on grounded systems and circuit ground to product shields near switches on ungrounded systems. This will help in establishing a common ground for the placement of the TVS diode.

ESD is characterized as a common-mode (line-to-ground) event. If there is an analog ground different from a digital ground, they may be connected together with a ferrite bead, capacitor or a low voltage TVSD.

## SUMMARY

A designer must acknowledge that real-world ESD events do occur and that the current ESD standards represent a minimum level of protection. While manufacturers may incorporate measures to reduce the effects of ESD during the manufacturing process, this does little good to reduce the effects of ESD caused by the end-user. It is important to employ protection components that will meet the standard as well as real-world ESD threats. With proper selection and placement of TVS diodes, circuit designers can reduce the effects of ESD as well as other harmful transients.

## FOOTNOTES

1. "Key Considerations for ESD Circuit Protection", James Colby, Littelfuse, Inc., Electronic Design, September 3, 2001, Pages 64-70.
2. "Is ESD Still a Problem", Michael J. Brandt, Circuits Assembly, November 2001, Page 24.
3. "ESD Case History Immunizing a Desktop Business Machine", J.L.N. Violette, PhD & M.F. Violette, EE, ECM Technology, May-June 1986, Pages 55-60.
4. IEC 61000-4-2 (1995-05), Electromagnetic Compatibility (EMC) - Part 4-2: Testing and Measurement Techniques - Electrostatic Discharge Immunity Test, International Electrotechnical Commission, Geneva, Switzerland.
5. "Triboelectric Generation: Getting Charged", Ryne C. Allen, Evaluation Engineering, November 2000, Pages S-4 to S-10. "Triboelectric Charge: Its ESD Ability and a Measurement Method for its Prosperity on Packaging Materials", J.R. Huntsman, EOS/ESD Symposium Proceedings, EOS-6, 1984, Pages 64-77.
6. The first was resistance of the human body, the storage capacitor and the current waveform.
7. The actual value for each of these standards can be found in tables within the individual documents. It is not the purpose of the article to list those specific classes, test, voltages and peak pulse currents.
8. "Spark Initiation Requirements of a Secondary Explosive", T.J. Tucker, Sandia Laboratory, Alt New Mexico, Annals of New York Academy of Science, Volume 152, Article 1, Pages 643-653, October 28, 1968, SC-R-68-1759.

## COMPANY INFORMATION

### COMPANY PROFILE

ProTek Devices, based in Tempe, Arizona USA, is a manufacturer of Transient Voltage Suppression (TVS) products designed specifically for the protection of electronic systems from the effects of lightning, Electrostatic Discharge (ESD), Nuclear Electromagnetic Pulse (NEMP), inductive switching and EMI/RFI. With over 25 years of engineering and manufacturing experience, ProTek designs TVS devices that provide application specific protection solutions for all electronic equipment/systems.

ProTek Devices Analog Products Division, also manufactures analog interface, control, RF and power management products.

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