ETHERNET LAYOUT SUGGESTIONS USING PROTEK DEVICES' PARTS

This brief is to assist the design engineer in the placement of Protek Devices various parts for the protection of Ethernet applications against the effects of Electrostatic Discharge (ESD) and secondary lightning. The placements are for illustration purposes only, as the PCB engineer may have tighter geometries that are not shown in the below drawings.

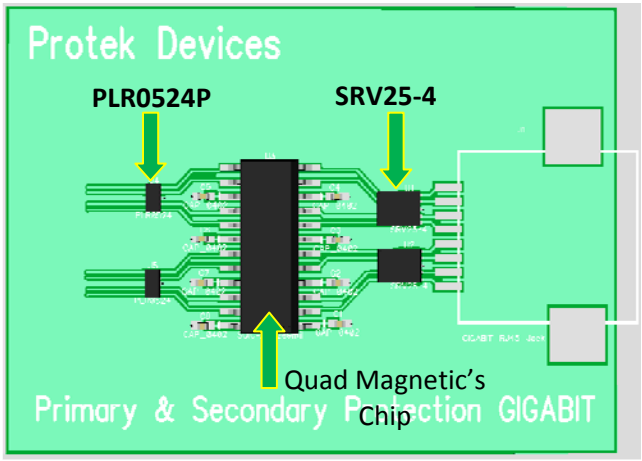

Figure 1 - Primary and Secondary Protection Using the PLR0524P & SRV25-4

In order to meet the regulatory requirements of IEC 61000-4-5, GR 1089-CORE, FCC Part 68, UL497B and ITU-T K20 and K21, the protector should be able to withstand over voltages that exceed 1,500 Volts and surge currents up to 100Amps (8/20µs, 10/1000µs or 10/700µs surge waveforms).

Data line protection elements are normally required on both the line-side (primary) and chip-side (secondary) of the line transformers. Line-side suppression diverts the build-up of the transient current, thus protecting the transceiver as well as the transformer. Chip-side protection protects the transceiver IC from fast transient events that are coupled through the transformer due to parasitic winding capacitance.

As shown in Figure 1, for primary (line-side) protection the SRV25-4 is recommended and for secondary (chip-side) protection after the magnetic transformers that provide 1,500 Volts of isolation, the PLR0524P is recommended. The traces maintain the 90Ω differential specification for high speed data transfer typical for Gigabit Ethernet applications. To minimize the path length between the protection devices and the lines, place the TVS diodes close to the RJ-45 connector and the terminal of the isolation transformer to restrict transient coupling to nearby traces. The total voltage from the IC chips on the equipment side will be the combination of the TVS clamping voltage and the overshoot voltage due to wire inductance. It is important to make trace inductance as small as possible.

Grounding is another concern. Lightning is a common-mode transient, which is referenced to a low impedance ground such as a chassis or a PCB ground plane. A low impedance grounding system (less than 0.5 Ohms) with minimum discontinuities is important for optimal design layout.

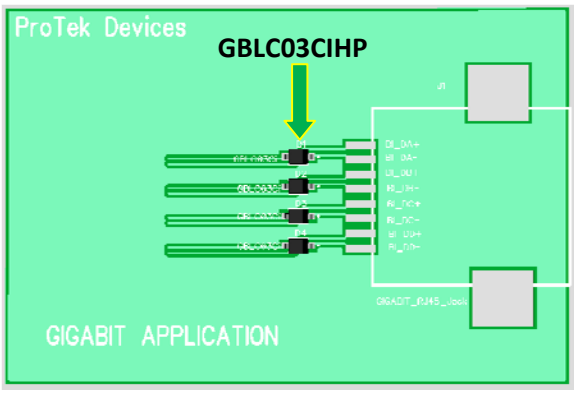

Figure 2 - Gigabit Protection Using the GBLC03CIHP

As shown in Figure 2, the GBLC03CIHP is used in a differential-mode between each of the 4 positive and negative data pairs (D+, D-) in a Gigabit application. The data pair traces are 7mil wide with 7mil spacing. With the PCB dielectric of 5.6, this will provide 90Ω differential traces. The traces maintain the same separation even through the connection of the pads of the GBLC03CIHP. The TVS device is connected as close as possible to the RJ-45 connector to minimize the inductance of the traces.

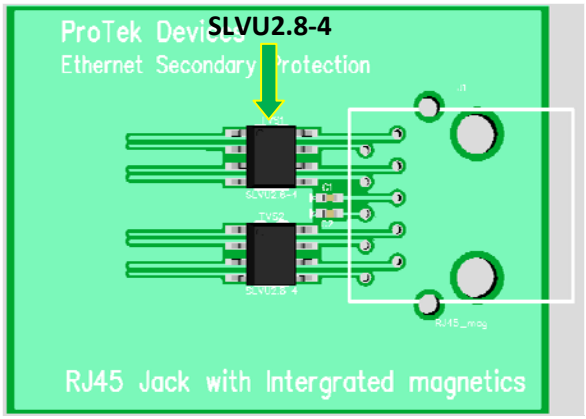

Figure 3 - Ethernet with Integrated Magnetic Connector Using the SLVU2.8-4

As shown in Figure 3, the SLVU2.8-4 is used in differential-mode and connected to an integrated magnetic RJ-45 connector. The same 90Ω differential criterion applies in this application as before. The SLVU2.8-4 has a feed through design providing bidirectional protection for each data pair (Pin 1 to Pin 8 and Pin 2 to Pin 7) for an application where integrated magnetics and RJ-45 plugs are used. The TX RX data pulses are normally 2.5V (Peak). The SLVU2.8-4, with the I/O to ground capacitance of less than 3.0pF is the ideal device for protecting the down-stream PHY.

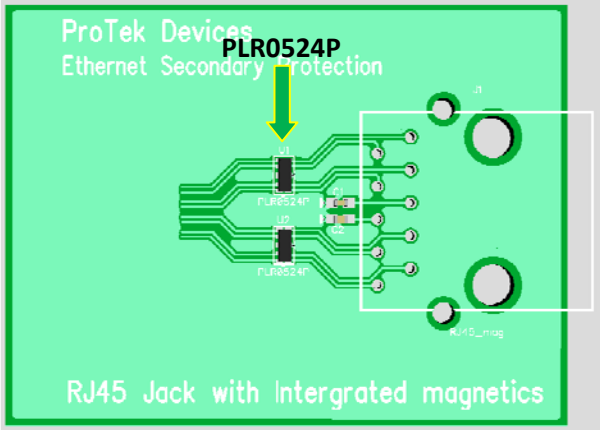

Figure 4 - Integrated Connector Using the PLR0524P

As shown in Figure 5, the PLR0524P is used in the same integrated connector Ethernet application as shown previously. The PLR0524P is a smaller packaged device thereby saving on costly PCB real estate.

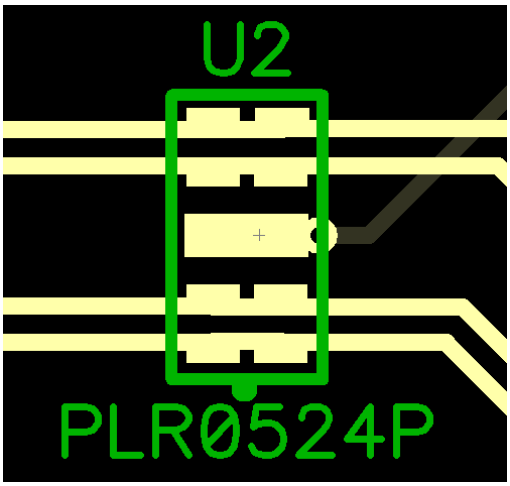

Figure 5 - Enlarged View of the PLR0524P

The enlarged view of the PLR0524P (Figure 5) shows the flow through design of the package. The center pad is the ground pad which will be used for common-mode protection. For differential-mode protection the ground pad is not connected