HDMI LAYOUT SUGGESTIONS USING PROTEK DEVICES' PARTS

This brief is to assist the design engineer in the placement of Protek Devices various parts for the protection of HDMI applications against the effects of Electrostatic Discharge (ESD) and secondary lightning. The placements are for illustration purposes only, as the PCB engineer may have tighter geometries that are not shown in the below drawings.

The High-Definition Multimedia Interface (HDMI) combines a high-speed unidirectional TMDS data link with low speed, bidirectional control and status links (DDC and CEC) and configuration protocols in a single user-friendly high performance connector.

The high-performance digital imaging silicon ASICs required for these applications usually include some protection sufficient for a controlled manufacturing environment. But the fabrication geometry has been optimized for performance, not ruggedness, and is no match for the uncontrolled ESD environment of the end-user. Therefore, even the most basic HDMI port implementation for these applications necessarily entails multiple external interface and protection circuits. Any I/O signal exposed to the outside world ESD strikes are in constant danger during interconnection. A single spark can render an entire entertainment system useless.

Each TMDS line is protected from ESD with a low-capacitance steering diode pair that routes negative ESD pulses directly into ground and positive pulses back to ground through a TVS diode. Each of the signal lines exposed to the HDMI connector are protected in this manner as shown in Figure 1.

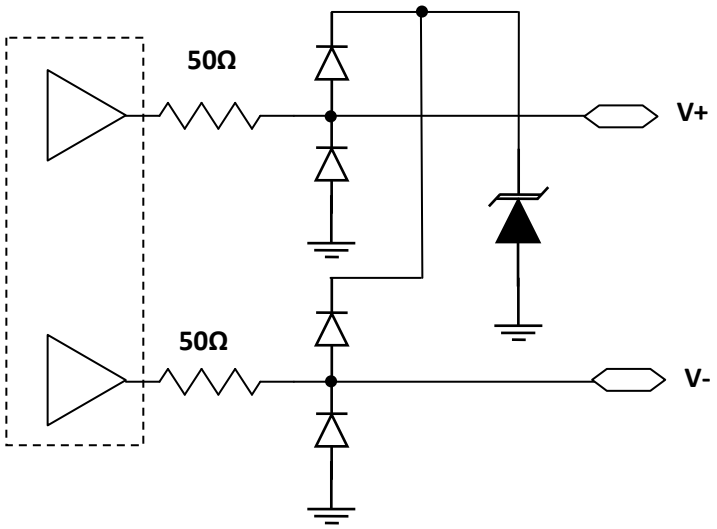

Figure 1 - TMDS Pair Protected by Using the PLR0524P

In order to meet both the signal integrity and the ESD immunity requirements, the chosen protection device should have as small of a capacitance value as possible, preferably less than 0.6pF. This is because the lower the protection device's capacitance, the less the device will affect the differential line impedance when it is added to

the HDMI layout. To further facilitate the high-speed design, the protection device should also offer flow-through, symmetrical layout capability. Symmetrical and uninterrupted signal layout will help maintain the signal integrity by streamlining high-speed signal line design and maintain impedance requirements.

In addition to the electrical characteristics requirement, to ensure maximum reliability for the HDMI ASIC, the same protection device should provide repeatable ESD immunity to and beyond level 4, IEC 61000-4-2 to each of the exposed signal pins. In other words, when testing the I/O or power pin of the HDMI connector, each pin should have a minimum of ±8kV contact ESD and ±15kV air ESD handling capability when surged directly with ESD. The PLR0524P is just such a device.

HDMI Applications Layout

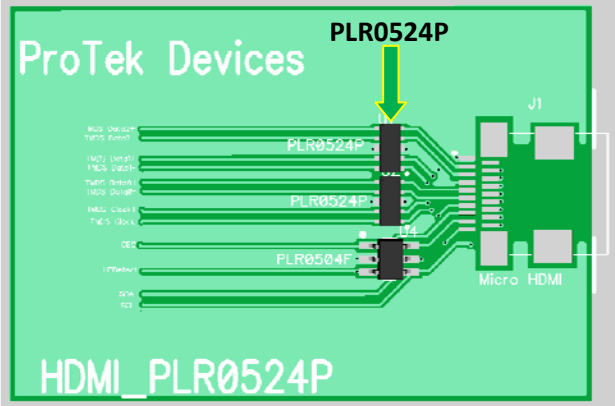

Figure 2 – TDMS Data Line and Clock Protection Using the PLR0524P

As shown in Figure 2, PLR0524P is used to protect the TMDS Data lines and the Clocks. The HP Detect, SDA, SCL and CEC are protected by the PLR0504P. The PLR0504F is used as the reference pin is connected to the V_{CCBUS} to protect from any surges and ESD threats that may be present when plugging in the HDMI connector.

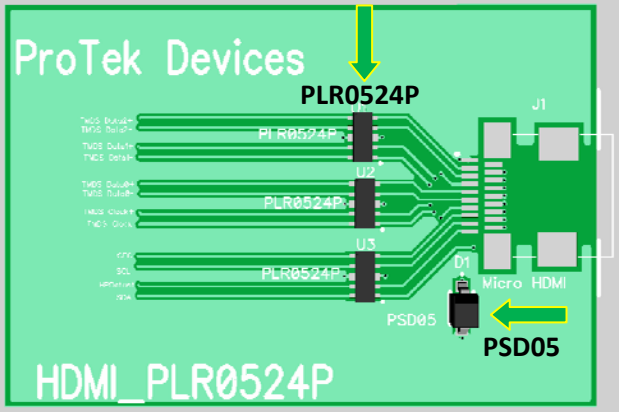

Figure 3 – Data Line & V_{CCBUS} Protection Using the PLR0524P and the PSD05

As shown in Figure 3, three of the PLR0524P are used to protect all the data lines and a PSD05 is added to protect the V_{CCBUS}. The PSD05 is a good choice as there are large inductive surges when plugging in the connector. This device has a good clamping ability with a 500 Watt surge suppression using the IEC 61000-4-5 secondary lightning specification of the 8/20µs surge waveform.